

1024 x 4-BIT STATIC CMOS RAM

DESCRIPTION

The μPD444 is a high-speed, low power silicon gate CMOS 4096 bit static RAM organized 1024 words by 4 bits. It uses DC stable (static) circuitry throughout and therefore requires no clock or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided.

\overline{CS} controls the power down feature. In less than a cycle time after \overline{CS} goes high — deselecting the μPD444 — the part automatically reduces its power requirements and remains in this low power standby mode as long as \overline{CS} is high. There is no minimum \overline{CS} high time for device operation, although it will determine the length of time in the power down mode. When \overline{CS} goes low, selecting the μPD444, the μPD444 automatically powers up.

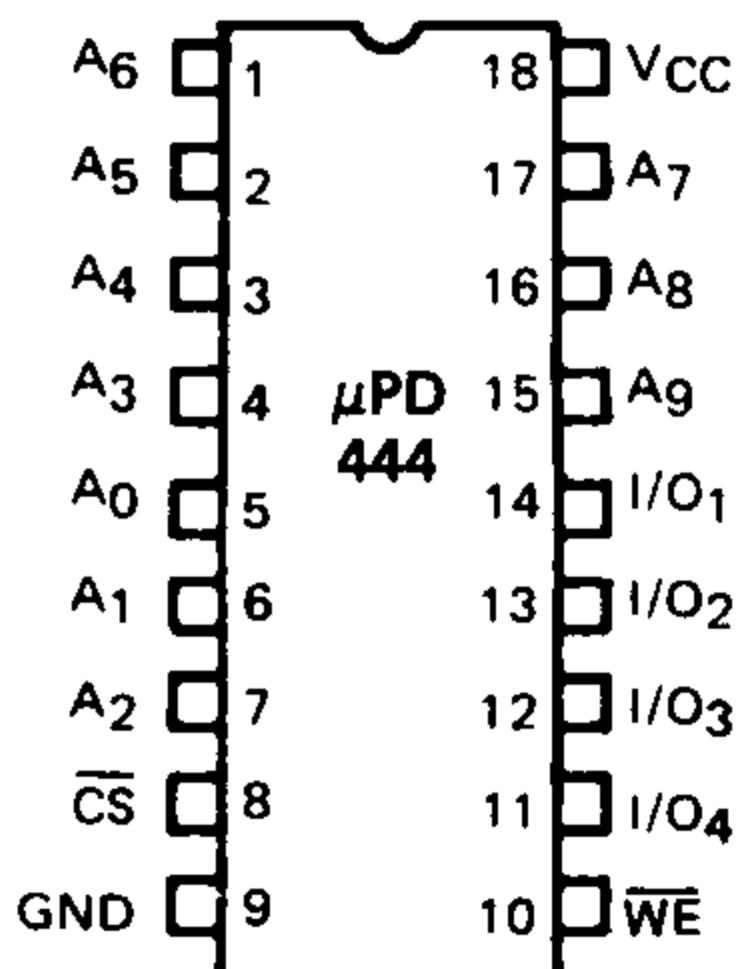
The μPD444 is placed in an 18-pin plastic package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The μPD444 is pin-compatible with the μPD2114L NMOS Static RAM.

Data retention is guaranteed to 2 volts on all parts. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility is required.

FEATURES

- Low Power Standby — 1 μA Typ.
- Low Power Operation
- Data Retention — 2.0V Min.
- Capability of Battery Backup Operation
- Fast Access Time — 200-450 ns
- Identical Cycle and Access Times
- Single +5V Supply
- No Clock or Timing Strobe Required
- Completely Static Memory
- Automatic Power-Down
- Directly TTL compatible: All Inputs and Outputs
- Common Data Input and Output using Three-State Outputs
- Available in a Standard 18-Pin Plastic Package
- For Operation at +3V Power Supply, Contact the NEC Sales Office.

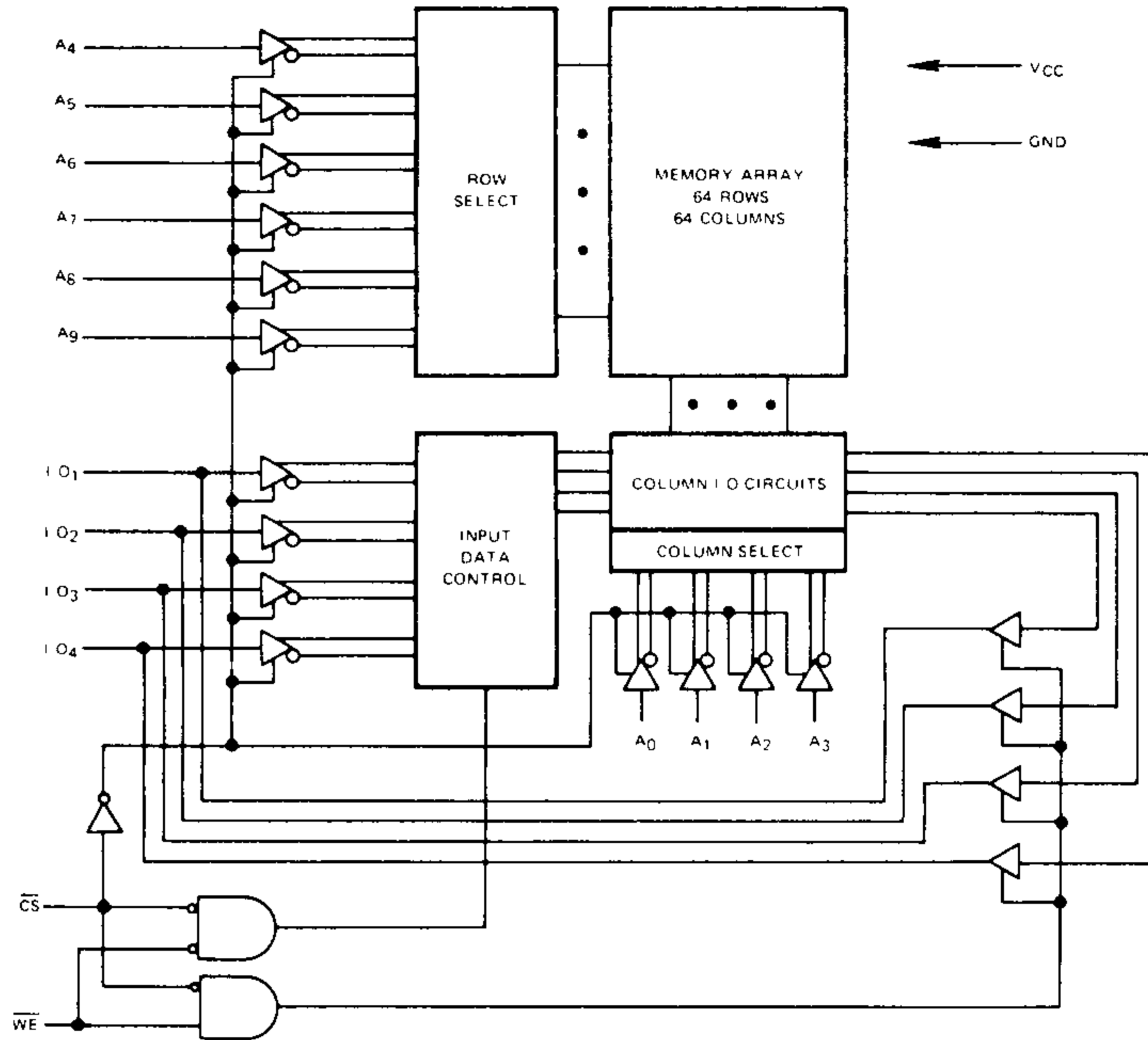
PIN CONFIGURATION



PIN NAMES

A ₀ -A ₉	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
I/O ₁ -I/O ₄	Data Input/Output
VCC	Power (+5V)
GND	Ground

Rev/2



BLOCK DIAGRAM

Operating Temperature -40°C to +85°C
 Storage Temperature -55°C to +125°C
 All Input and Output Voltages. -0.3 to V_{CC} +0.3 Volts ①
 Supply Voltage +8.0 Volts

ABSOLUTE MAXIMUM RATINGS*

Note: ① With Respect to Ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_a = -40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS												UNIT	TEST CONDITIONS
		444-3			444-2			444-1			444				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input Leakage Current	I _{LI}	-1.0		1.0	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	V _{IN} = GND to V _{CC}
I/O Leakage Current	I _{LO}	-1.0		1.0	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	$\overline{CS} = V_{IH}$, V _{I/O} = GND to V _{CC}
Operating Supply Current	I _{CCA1}		19	35		15	35		12	35		9	35	mA	$\overline{CS} = V_{IL}$, V _{IN} = V _{CC} , Outputs Open
Operating Supply Current	I _{CCA2}		23	40		19	40		15	40		12	40	mA	$\overline{CS} = V_{IL}$, V _{IN} = 2.4V, Outputs Open
Average Operating Supply Current	I _{CCA3}		10	20		9	20		8	20		7	20	mA	V _{IN} = GND or V _{CC} , Outputs Open f = 1 MHz, Duty 50%
Standby Supply Current	I _{CCS}		1	5		1	5		1	5		1	50	μA	$\overline{CS} = V_{CC}$, V _{IN} = GND to V _{CC}
Input Low Voltage	V _{IL}	-0.3		0.8	-0.3		0.8	-0.3		0.8	-0.3		0.8	V	
Input High Voltage	V _{IH}	2.4		V _{CC} + 0.3	2.4		V _{CC} + 0.3	2.4		V _{CC} + 0.3	2.4		V _{CC} + 0.3	V	
Output Low Voltage	V _{OL}			0.4			0.4			0.4			0.4	V	I _{OL} = 2.0 mA
Output High Voltage	V _{OH}	2.4			2.4			2.4					2.4	V	I _{OH} = -1.0 mA

T_a = 25°C, f = 1 MHz

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input/Output Capacitance	C _{I/O}			10	pF	V _{I/O} = 0V
Input Capacitance	C _{IN}			5	pF	V _{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

T_a = -40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS								UNIT	TEST CONDITIONS
		444-3		444-2		444-1		444			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE											
Read Cycle	t _{RC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts Input Rise and Fall Times: 10 ns Input and Output Timing Levels: 1.5 Volt Output Load: 1 TTL Gate and C _L = 100 pF
Address Access Time	t _{AA}		200		250		300		450	ns	
Chip Select Access Time ①	t _{ACS1}		200		250		300		450	ns	
Chip Select Access Time ②	t _{ACS2}		250		300		350		500	ns	
Output Hold from Address Change	t _{OH}	50		50		50		50		ns	
Chip Selection to Output in Low Z	t _{LZ}	20		20		20		20		ns	
Chip Deselection to Output in High Z	t _{HZ}		60		70		80		100	ns	
WRITE CYCLE											
Write Cycle Time	t _{WC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts Input Rise and Fall Times: 10 ns Input and Output Timing Levels: 1.5 Volt Output Load: 1 TTL Gate and C _L = 100 pF
Chip Selection to End of Write	t _{CW}	180		230		250		350		ns	
Address Valid to End of Write	t _{AW}	180		230		250		350		ns	
Address Setup Time	t _{AS}	0		0		0		0		ns	
Write Pulse Width	t _{WP}	180		210		230		300		ns	
Write Recovery Time	t _{WR}	0		0		0		0		ns	
Data Valid to End of Write	t _{DW}	120		140		150		200		ns	
Data Hold Time	t _{DH}	0		0		0		0		ns	
Write Enabled to Output in High Z	t _{WZ}		60		70		80		100	ns	
Output Active from End of Write	t _{OW}	0		0		0		0		ns	

Notes: ① Chip deselected for greater than 100 ns prior to selection.
② Chip deselected for a finite time that is less than 100 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

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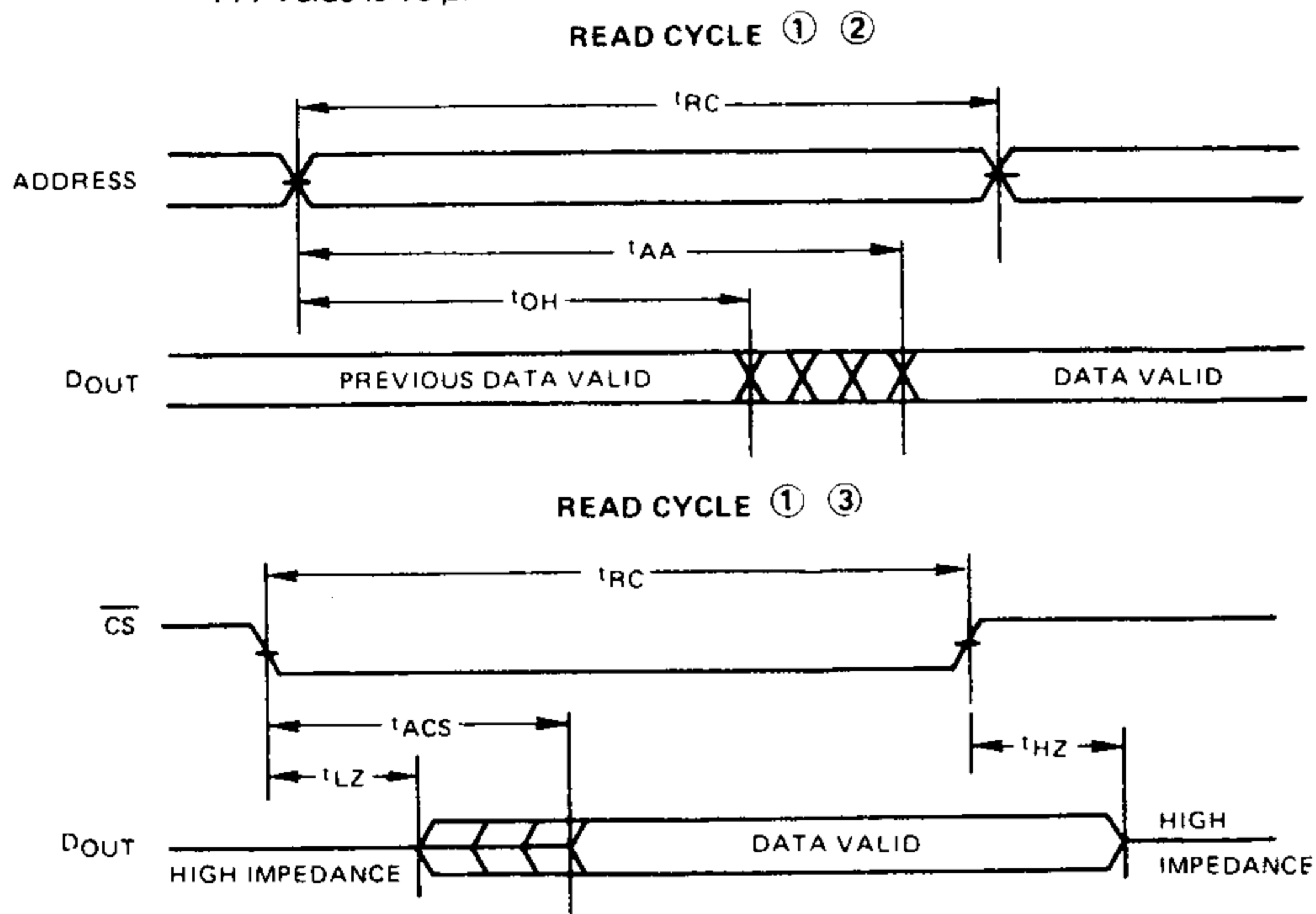
LOW V_{CC} DATA RETENTION CHARACTERISTICS

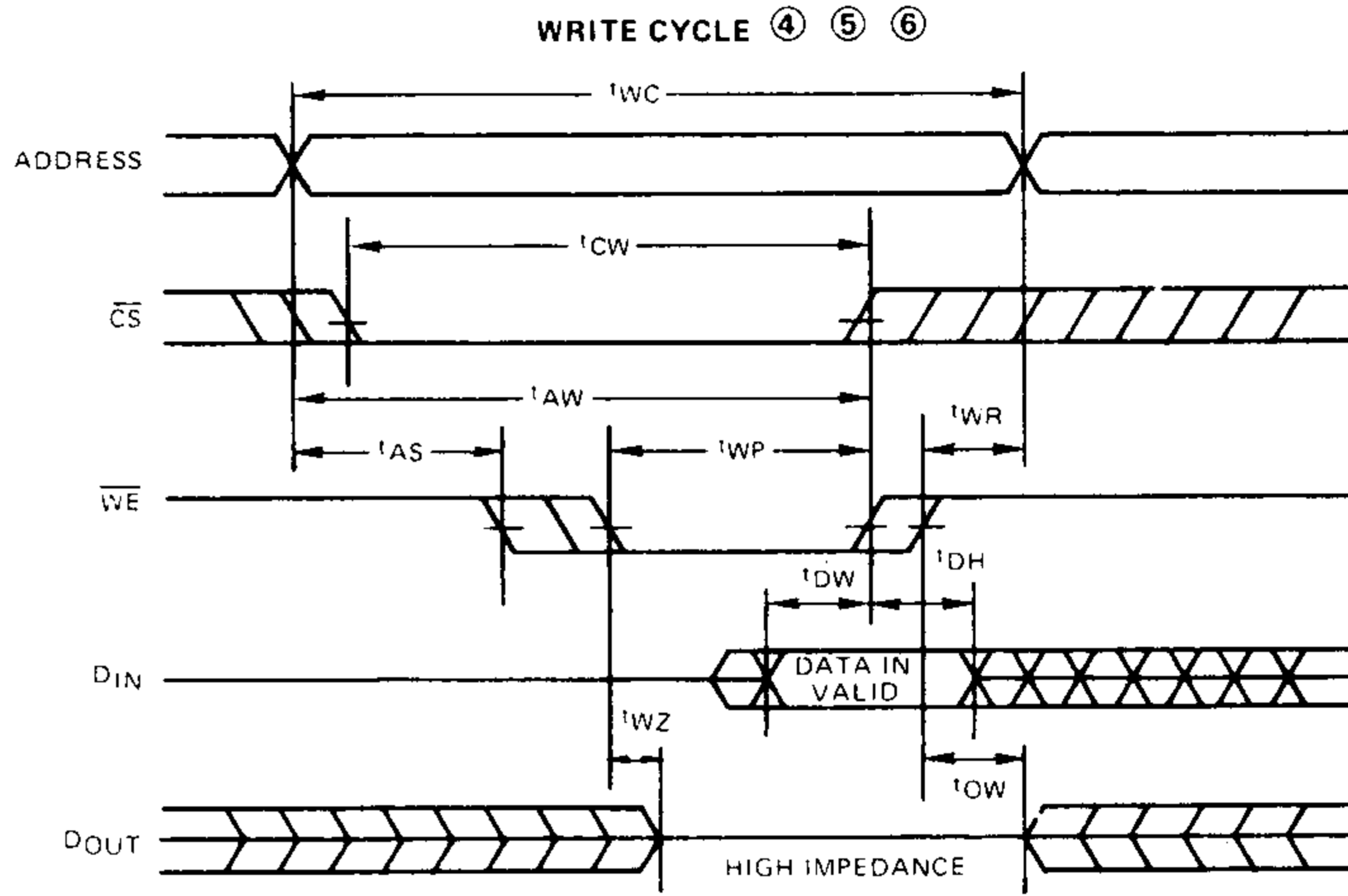
T_a = -40°C to +85°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Data Retention Supply Voltage	V _{CCDR}	2.0			V	$\overline{CS} = V_{CC}, V_{IN} = V_{CC}$ to GND
Data Retention Supply Current	I _{CCDR}		0.01	②	μA	V _{CC} = 3V, $\overline{CS} = V_{CC}$ V _{IN} = V _{CC} to GND
Chip Deselect to Data Retention Time	t _{CDR}	0			ns	
Operation Recovery Time	t _R	t _{RC} ①			ns	

Notes: ① t_{RC} = Read Cycle Time
② 444-1, -2, -3: Value is 2 μA
444 Value is 10 μA

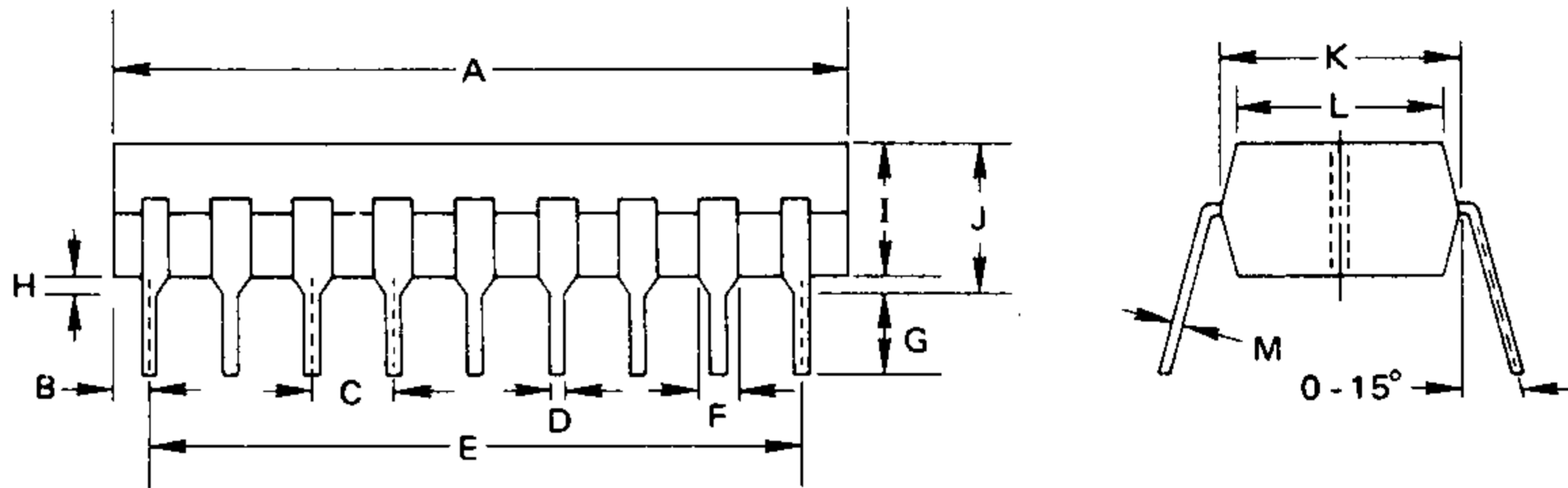
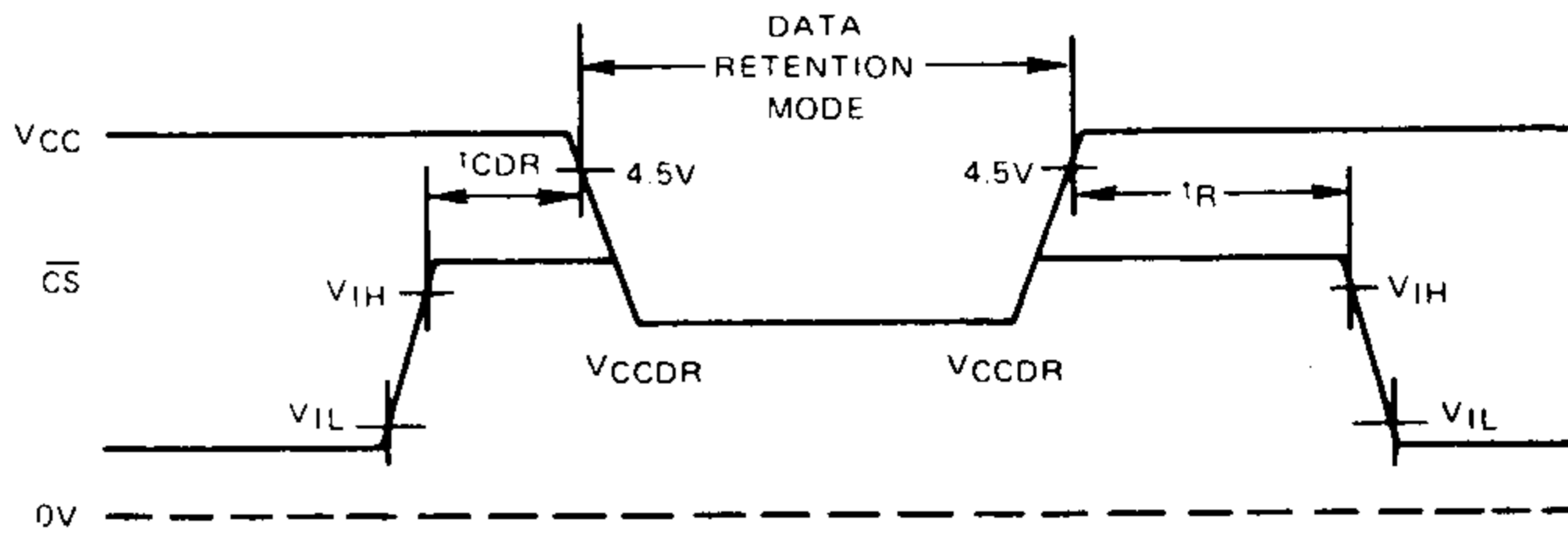
TIMING WAVEFORMS





- Notes:
- ① \overline{WE} is high for Read Cycles.
 - ② Device is continuously selected, $\overline{CS} = V_{IL}$.
 - ③ Address valid prior to or coincident with \overline{CS} transition low.
 - ④ If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition, the output buffers remain in a high impedance state.
 - ⑤ \overline{WE} must be high during all address transitions.
 - ⑥ t_{WP} is measured from the latter of \overline{CS} or \overline{WE} going low to the earlier of \overline{CS} or \overline{WE} going high.

LOW VCC DATA RETENTION



PACKAGE OUTLINE
μPD444C

Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01