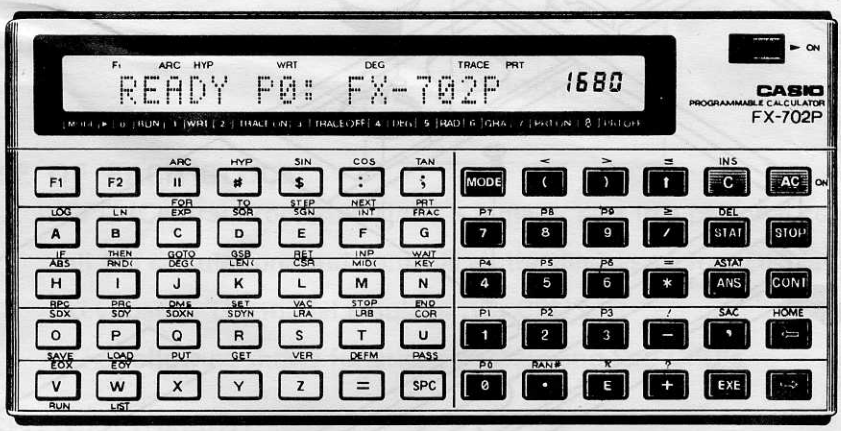
TEXTBOOK

FX702P (GX-272AA)

MAY.1982



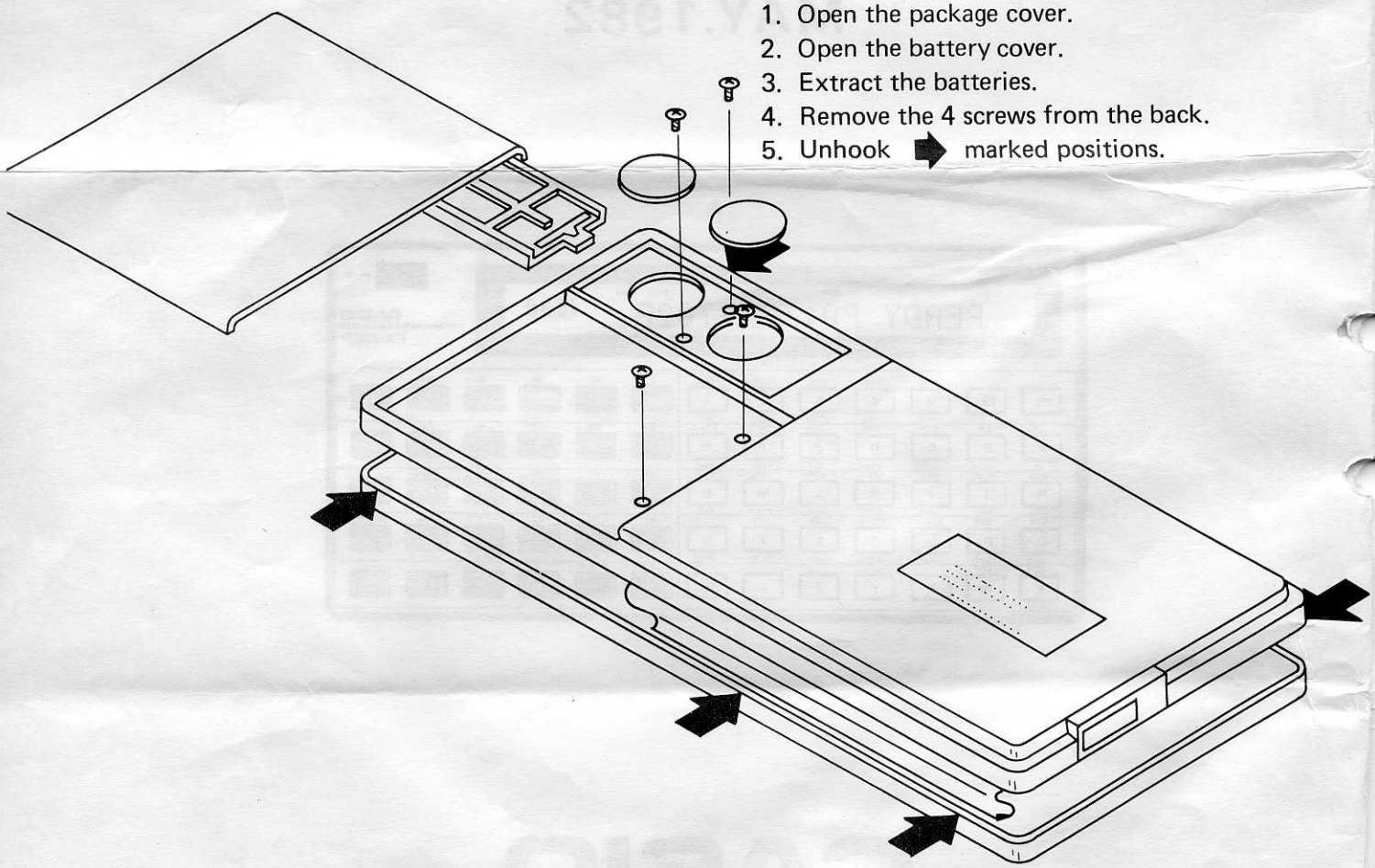
CASIO®

1. MAJOR SPECIFICATIONS

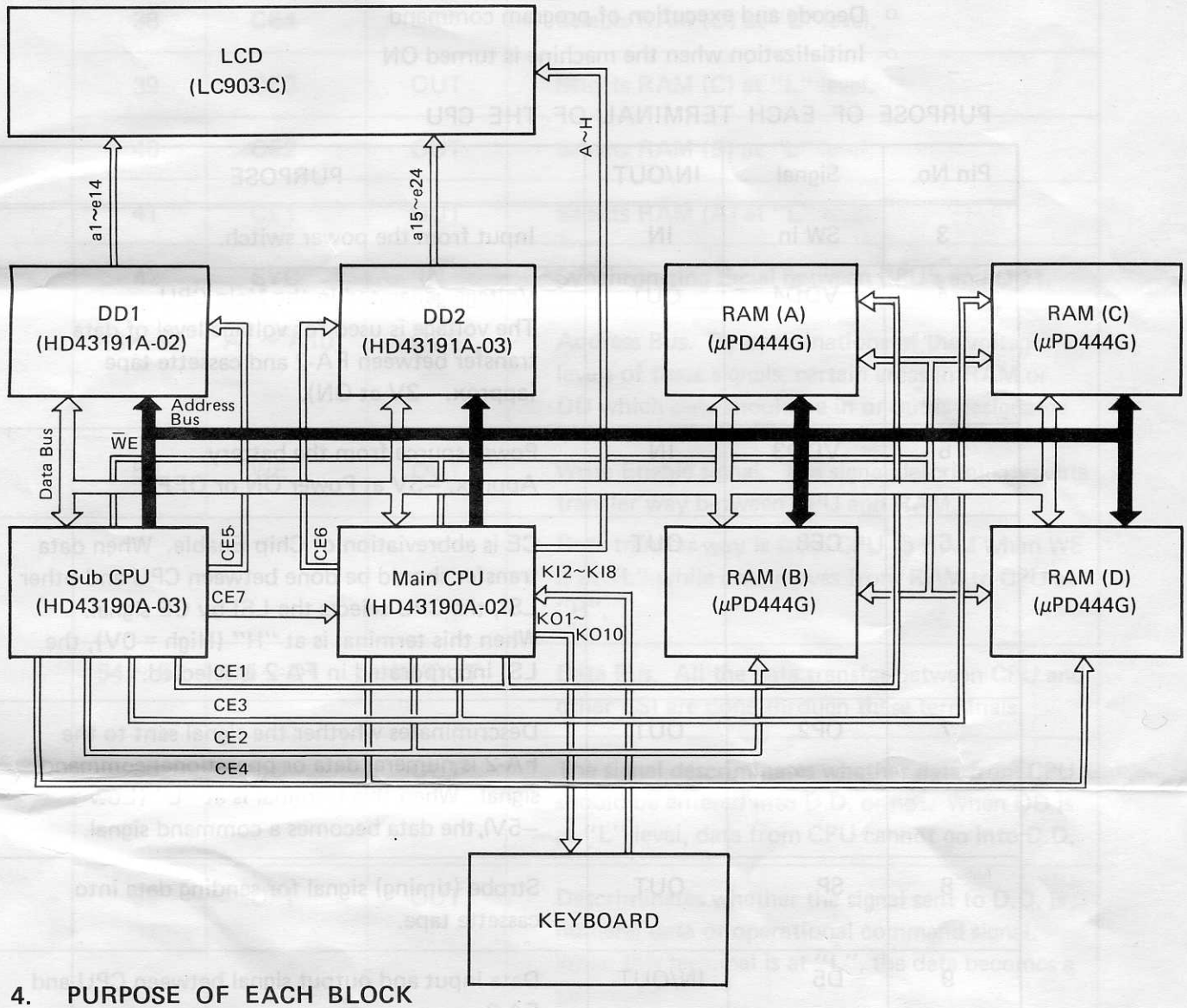
Calculation range :	$\pm 1 \times 10^{-99}$ to $\pm 9.999999999 \times 10^{99}$ and 0 Internal calculation uses 12 digit mantissa.
Program system :	Stored system
Program language :	BASIC
Number of steps :	80 to maximum of 226 steps (with power back-up)
Number of memories :	26 to maximum of 226 memories plus exclusive character variable $ (with power back-up)
Power source :	2 lithium batteries (CR-2032)
Power consumption :	0.01W (Max.)
Battery life :	The unit gives approximately 240 hours (approx. 200 hours with optional equipments) continuous operation on type CR2032.

2. DISASSEMBLY

1. Open the package cover.
2. Open the battery cover.
3. Extract the batteries.
4. Remove the 4 screws from the back.
5. Unhook ➡ marked positions.



3. BLOCK DIAGRAM



4. PURPOSE OF EACH BLOCK

4-1. CPU . . . . . CPU (Central Processing Unit) is a major part in a personal computer as it performs all the calculations and controls all the devices such as Display Drivers, RAM's and keyboard. The model employs two CPU's.
The following shows functions of Main and Sub CPU's.

Main CPU (HD43190A02)

- ○ Generates VDD2, VDD4 and Clock pulses Ø1, Ø2.
- ○ Decode and execution of program command.
- ○ Key input transaction.
- ○ Display transaction.
- ○ Cassette tape transaction.

SUB CPU (HD43190A03)

- Calculations
- Decode and execution of program command
- Initialization when the machine is turned ON

PURPOSE OF EACH TERMINAL OF THE CPU

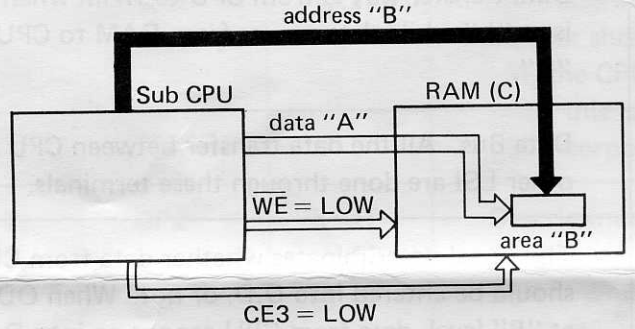
Pin No.	Signal	IN/OUT	PURPOSE
3	SW in	IN	Input from the power switch.
4	VDD4	OUT	Voltage generated in the Main CPU. The voltage is used for voltage level of data transfer between FA-2 and cassette tape (approx. –3V at ON).
5	VDD3	IN	Power source from the battery. Approx. –3V at Power ON or OFF
6	CE8	OUT	CE is abbreviation of Chip Enable. When data transfer should be done between CPU and other LSI, the CPU selects the LSI by CE signal. When this terminal is at "H" (High = 0V), the LSI incorporated in FA-2 is selected.
7	OP2	OUT	Descriminates whether the signal sent to the FA-2 is numeral data or operational command signal. When this terminal is at "L" (Low = –5V), the data becomes a command signal.
8	SP	OUT	Strobe (timing) signal for sending data into cassette tape.
9	D5	IN/OUT	Data input and output signal between CPU and FA-2.
10 ~ 17	KI1~KI8	IN	Key input terminals.
18 ~ 27	KO1~KO10	OUT	Key common signals.
28 ~ 30	B, D, F	OUT	Display signals.
35	CE7		When the Main CPU cannot perform a transaction, the Main CPU selects the Sub CPU by this terminal. When the signal is at "L" level, Sub CPU is designated.
36	CE6	OUT	Selects DD (Display Driver) 1 at "L" level.

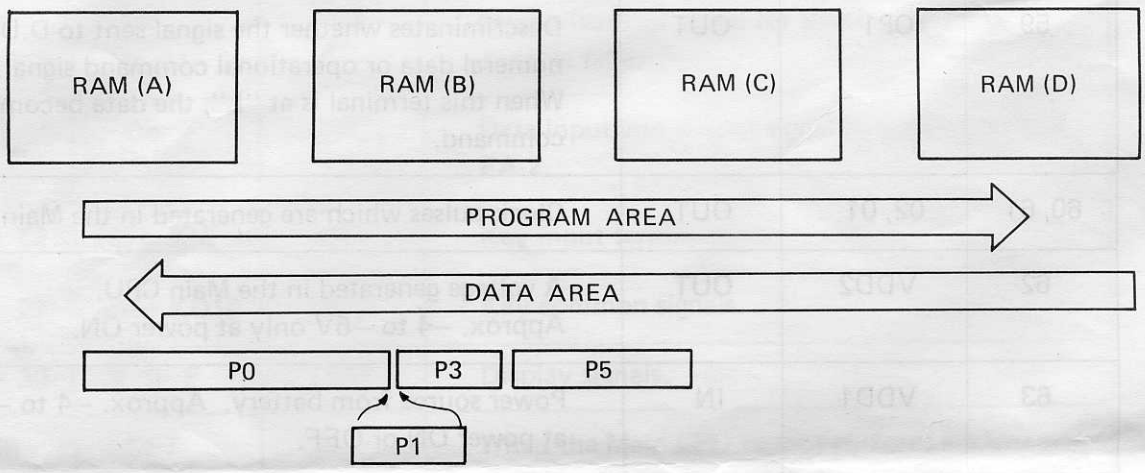
37	CE5	OUT	Selects DD2 at "L" level.
38	CE4	OUT	Selects RAM (D) at "L" level.
39	CE3	OUT	Selects RAM (C) at "L" level.
40	CE2	OUT	Selects RAM (B) at "L" level.
41	CE1	OUT	Selects RAM (A) at "L" level.
42	SYC	IN	Synchronizing signal between CPU's and DD1.
43 ~ 52	A1 ~ A10	OUT	Address Bus. By combinations of the voltage levels of these signals, certain areas in RAM or DD which data should be in or out is designated.
53	$\overline{WE}$	OUT	Write Enable signal. The signal descriminates data transfer way between CPU and RAM. Data transfer way is from CPU to RAM when $\overline{WE}$ is at "L" while data moves from RAM to CPU at "H".
54 ~ 57	D4 ~ D1	IN/OUT	Data Bus. All the data transfer between CPU and other LSI are done through these terminals.
58	OD	OUT	The signal descriminates whether data from CPU should be entered into D.D. or not. When OD is at "L" level, data from CPU cannot go into D.D.
59	OP1	OUT	Descriminates whether the signal sent to D.D. is numeral data or operational command signal. When this terminal is at "L", the data becomes a command.
60, 61	02, 01	OUT	Clock pulses which are generated in the Main CPU.
62	VDD2	OUT	A voltage generated in the Main CPU. Approx. −4 to −6V only at power ON.
63	VDD1	IN	Power source from battery. Approx. −4 to −6V at power ON or OFF.
64	V4	IN	Voltage level for display signals.
65 ~ 69	G ~ H	OUT	Display signals.
70, 71	V1, V3	IN	Voltage levels for display signals.

72, 73	OSI, OSO	IN/OUT	On this model, an 18K ohm resistor is connected between these terminals. By this resistance, frequency of the clock pulse is chosen.
74	SH	IN	Input terminal of schmitt trigger which initializes the machine at power switch is turned on.

4-2. RAM

RAM (Random Access Memory) is an element which stores data. RAM μPD444 has a capacity of 4K bit (4,096 areas of storing data). A data area is selected by the combinations of signals A1 to A10 from the CPU (selecting a data area is so called "addressing"). Data (combinations of voltage levels of signals D1 to D4) is inputted in or outputted from the selected area. Signal $\overline{WE}$ from the CPU descriminates whether the data should be read or written. When the signal $\overline{WE}$ is at "L" level, a data is read from a RAM to the CPU while data is written into RAM from CPU at "H" level. The model employs four RAM's and each RAM is designated by the signals CE1 to CE4 from the CPU. The left figure explains the idea that the Sub CPU writes data "A" into area "B" of the RAM (C). First, RAM (C) is designated by the signal CE3 and by signals A1 to A10, area "B" is selected. Data "A" is written into the area "B" through D1 ~ D4 terminals while $\overline{WE}$ is at "L" level.





The above figure shows entering method of program and data. Program enters from left [RAM (A)], data [such as A, B, C . . . Z, A$, B$, C$ . . . Z$, A (0) to A (199)] enters from right [RAM (D)]. The left of program area occupies the area of 160 characters (1 character =

1 byte, 1 byte = 8 bit) and is for input buffer*, object buffer* and $ code for character variable. Entering order of program is by the program number. For example, when programs P0, P3, P5 are in the machine and if program P1 is newly added, P1 intrudes between P0 and P3, P3 and P5 shift to the right.

*input buffer : Stores input key code temporarily.

*object buffer : Stores object code which is encoded from key code to calculation code.

4-3. DD and LCD

The main function of DD (Display Driver) is to convert data from CPU to display signals. DD's also help CPU's to program calculations. The model employs two DD's HD43191A03 and HD43191A02. HD43191A03 mainly controls the right half of display while HD43191A02 controls the left half.

The following lists the contents of each DD.

HD43191A02

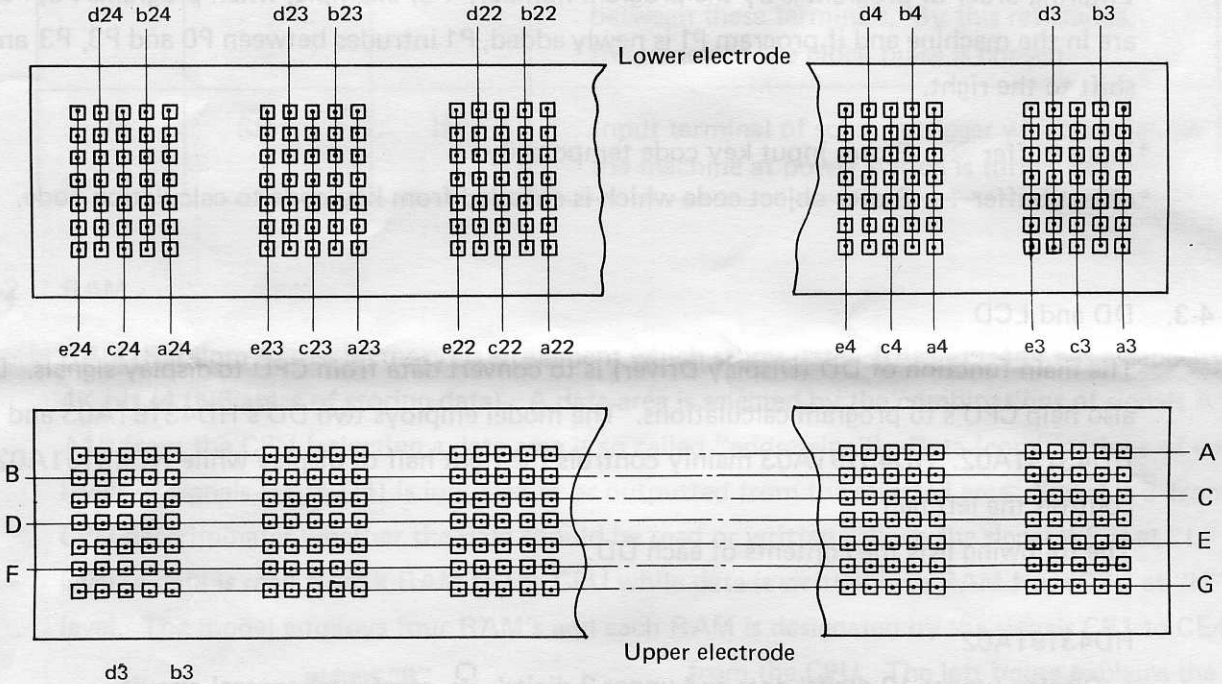
- Display (upper 10 digits' dots and upper 2 digits' 8 segments) control circuit.
- Calculation RAM.
- Constant ROM (stores constant number such as π = 3.1415 . . .).
- Key code decoding ROM (Decodes from key input code to internal calculation code).
- READY, ERROR message ROM.

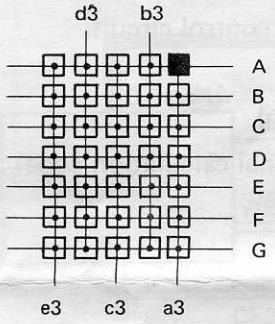
HD43191A03

- Display (lower 10 digits' dots and lower 2 digits' 8 segments) control circuit.
- Function name (such as SIN, COS, TAN . . .) and command name (such as FOR, NEXT, PRT . . .) displaying ROM.
- Display buffer.
- Pointer (storage register which keeps return address when a program is jumped to a subroutine) RAM and others.

*ROM : Abbreviation of Read Only Memory. An element of which data is only read while RAM is able to read or write data.
Namely, ROM is to be compared to a book while RAM is to be compared to a black board which you can write and read freely.

Method of dot displaying





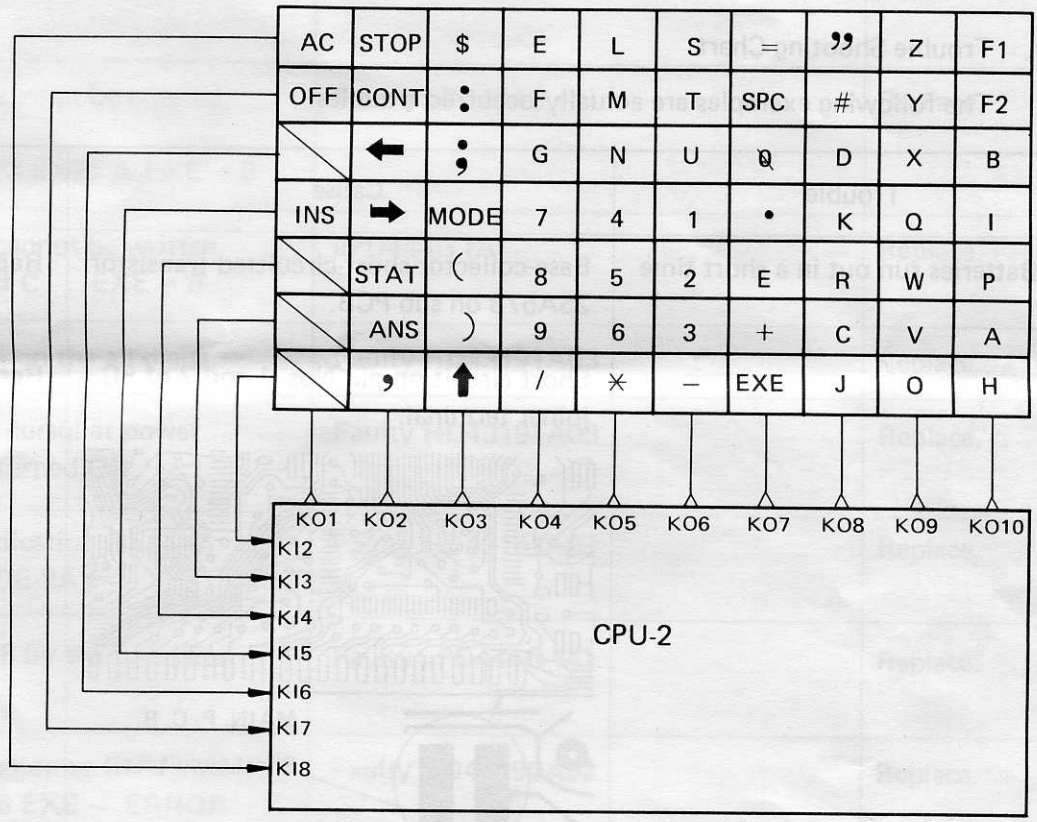
Numbers and characters are displayed in 5x7 dots.

On the upper electrode of the LCD, common signals A to G are applied horizontally while signals a3~e3 to a24~e24 are applied vertically on the lower electrode. On the left figure of the front page, the upper right corner of the dots is displayed when there is a voltage difference between signals A and a3. The signals A to G are generated in the Main CPU while signals a1~e1 to a24~e24 are generated in the two DD's.

4-4. KEYBOARD

Keyboard data communications are made between the Main CPU and the keyboard. The following shows the keyboard matrix of model FX-702P. Key common signals KO1~KO10 are generated from the Main CPU and always applied into the keyboard.

If a key is hit, corresponding key common signal is applied from a certain key input terminal of the Main CPU so that the CPU descriminates which key is hit.



If the key "1" is hit, the key common signal KO6 enters into the CPU-2 from the KI5 terminal.

4-5. POWER SUPPLY

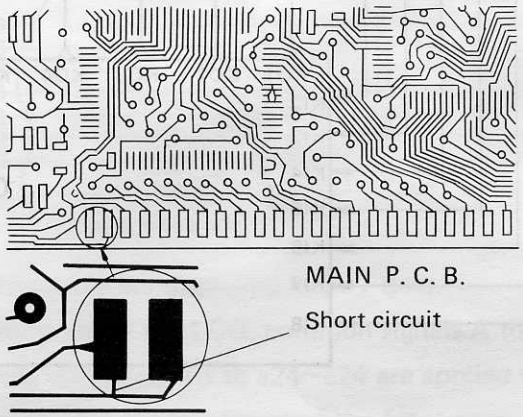
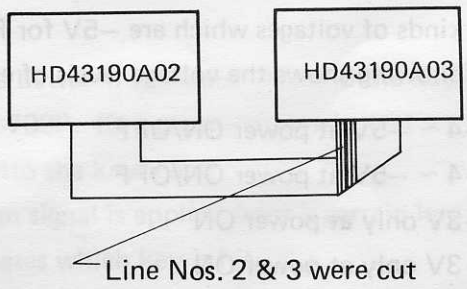
There are two kinds of voltages which are −5V for FX-702P circuit and −3V for FA-2, FP-10 circuits. The following shows the voltage levels of each power supply.

- VDD1 : −4 ~ −5V at power ON/OFF
- VDD2 : −4 ~ −5V at power ON/OFF
- VDD2 : −3V only at power ON
- VDD4 : −3V only at power ON

5. REPAIR

5-1. Trouble Shooting Chart

The following examples are actually occurred troubles.

Trouble	Cause	Solution
Batteries run out in a short time	Base-collector short-circuitted transistor 2SA573 on sub PCB.	Replace the transistor.
	Short circuit on pin Nos. 1 and 2 of PC joiner terminal. 	Remove the solder.
ANS key does not move smoothly.	There was an earth spring between contact rubber and key.	Remove the earth spring.
Shows ERROR by RUN START Example: RUN → ERROR IN PØ XX	Cut line of PCB jumper cable. 	Replace the PCB jumper.
Funny indication	Short circuit between pins 62 & 63 of HD43191A03.	Desolder.
No display at all	Cut P.C. joiner.	Replace.
No display at all (slightly seen from below)	Poor soldering of HD43190A03.	Resolder.
No display (Sometimes)	Poor contact of power switch	Clean & adjust.

ANS, CURSOL keys cannot be entered.	Keyboard PCB line cut.	Wired.
Variable cannot be entered. Example: A=123 EXE, A EXE → Ø	Faulty μPD444G (D)	Replace.
Program cannot be written. A=B * C EXE → Ø	μPD444G (A)	Replace.
Shows ___ on the all digits.	Faulty HD43191A03	Replace.
Shows an cursol at power switch is turned ON.	Faulty HD43191A03	Replace.
Funny indication READY PØ → RHDE-PA	Faulty HD43191A02	Replace.
Shows 678 by the operation MODE 1	Faulty μPD444G (A)	Replace.
No calculation at RUN mode. 123 + 456 EXE → ERROR	Faulty HD43190A02	Replace.
No calculation at RUN mode. 123 + 456 → 123 +	Faulty HD43190A03	Replace.

5-2. Function Check of Each LSI

A. Display

The following LSI's are functioning to display READY PØ at power switch is turned ON.

○ HD43190A02 ○ HD43190A03 ○ HD43191A02 ○ HD43191A03
○ μPD444G (A)

B. Key input

The following LSI's are functioning to enter numbers, characters, AC, ⇨ and ⇦ keys.

○ HD43190A02 ○ HD43191A02 ○ HD43191A03 ○ μPD444G (A)

C. Functions of RAM (B) to RAM (D) can be checked by entering a number into the following variables and reading the entered number.

○ RAM (B) : A (102) to A (165)
○ RAM (C) : A (35) to A (101)
○ RAM (D) : A to Z, A (1) to A (37)

NOTE: As normal memory for variables are only 26, increase the memory by using DEFM command.

[Example] Program for checking the function of RAM (B)

```
10 FOR I = 102 TO 165
20 A (I) = I
30 NEXT I
40 WAIT 5
50 FOR P = 102 TO 165
60 PRT A (P)
70 NEXT P
80 END
```

After writing the above program, increase the memory by the operation of DEFM 17 EXE. And if the display counts from 102 to 165 by RUN EXE, the RAM (B) is functioning properly.

5-3. Check Program

```
*** PRG LIST

VAR: 126 PRG: 880

P0: 118 STEPS
  10 A=9999999999:B=
     6666666666:C=A
  20 FOR I=0 TO 99:A
     (I)=99:A(I)=C:N
     EXT I:FOR I=0 T
     O 99
  30 IF A(I)≠C THEN
     ER
  40 NEXT I:IF C=A:C
     =B:GOTO 20
  50 GSB #2:PRT "ALL
      OK";:END

P2: 191 STEPS
 100 VAC
 200 IF "AB"="AB" TH
     EN 210
 205 GOTO 1
 210 IF "A"<"AB" THE
     N 220
 215 GOTO 1
 220 IF "AB">"A" THE
     N 230
 225 GOTO 1
 230 IF "01"≦"AB";IF
      "AB"≧"01" THEN
      240
 235 GOTO 1
 240 IF -123≠123:IF
     123<-123 THEN 1
 250 IF -1234>-123 T
     HEN 1
 260 IF -123≦-1234 T
     HEN 1
 270 IF 123≧456 THEN
      1
 280 IF 456=123 THEN
      1
 300 VAC :GOTO #3
```

```
P3: 269 STEPS
  10 IF RND(SIN 185+
     COS 230+TAN 1E-
     3+EXP 0,-5)≠0.2
     701 THEN 1
  20 A=DEG(30)+DEG(3
     0,59)+DEG(30,59
     ,60)
  30 A=A+12345*12345
     /234/345+SQR 0+
     SQR 2+SQR 30+-S
     IN -30↑2!
  40 A=A+AHS AHC AHT
      HTN HCS HSN 1+
     AHT HTN 1E-4
  50 FOR I=-5 TO 4:B
     =B+RND(5544.445
     55,I):NEXT I
  60 A(0)=1:A(0,0)=A
     (0)+1:A(0)=A(0,
     0)+(-3)↑3:B=B+A
     0
  70 RPC 3,5:V=X:W=Y
     :PRC 5,3:X=X+V:
     Y=Y+W
  80 SAC :STAT 3,5:S
     TAT 9,10:STAT 7
     ,8
  90 GOTO #4

P4: 92 STEPS
  10 M=123:N=456:0$=
     "M,N"
  20 $=0$+"=":$=MID(
     1,3)+MID(4)
  30 Z=CNT+MX+MY+SDX
     +SDXN+SDY+SDYN+
     LRA+LRB+COR+EOX
      5+EOY 3
  40 Z=Z+LEN($)
  50 GOTO #9
```

```
P9: 133 STEPS
  10 IF RND(A,-2)≠19
     87.4 THEN 1
  20 IF RND(B,-1)≠54
     737 THEN 1
  30 IF $≠"M,N=" THE
     N 1
  40 IF RND(X,-8)≠10
     .8240996 THEN 1
  50 IF RND(Y,-8)≠59
     .2979233 THEN 1
  60 IF RND(Z,-8)≠43
     .4193236 THEN 1
  70 IF RAN#≧1 THEN
     1
  80 RET
```

Save this program into a cassette tape by SAVE LOAD after increasing the memory by DEFM 10 EXE.

Checking Method

a. Necessary Equipments
   - ○ FX-702P to be checked
   - ○ FA-2
   - ○ Cassette tape recorder
   - ○ Cassette tape which contains the checking program

b. Connect FX-702P, FA-2 and a cassette tape recorder and load the program by the operation LOAD ALL EXE.

c. After loading, confirm that the remaining program steps are ØØ77.

d. Execute PØ.

e. If display shows ALL OK after about 48 seconds, the FX-702P is functioning properly.